

10/U31117

FILED UNDER 35 U.S.C. § 111

BEST AVAILABLE COPY

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10031117	FILING DATE 01/16/2002	CLASS 438	SUBCLASS 257	GAU 2827 2012	EXAMINER TRINH
**APPLICANTS: Kobayashi Takashi; Goto Yasushi; Kure Tokuo; Kurata Hideaki; Kume Hitoshi; Kimura Katsutaka; Saeki Syunichi;					
**CONTINUING DATA VERIFIED: THIS APPLICATION IS A 371 OF PCT/JP00/06140 02/08/2000					
** FOREIGN APPLICATIONS VERIFIED: JAPAN 11-257990 09/10/1999.					
PG-PUB <input type="checkbox"/>		DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>	
Foreign priority claimed		<input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO XA-9593	
35 USC 119 conditions met		<input type="checkbox"/> yes <input type="checkbox"/> no			
Verified and Acknowledged Examiners's initials					
TITLE : Integrated circuit and method of manufacture thereof					
U.S. DEPT. OF COM. / PAT. & TM-PTO-436L (Rev. 12-94)					

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G.
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs. Drwg.
<input type="checkbox"/> TERMINAL		Application Examiner		